

# Intel H61 MATX Schematic

## H61GV22D\_20120522

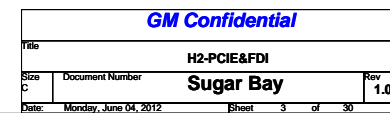
H61GV22D-在gv22C基础上VGA部分行场信号串电阻

Version: 1.0

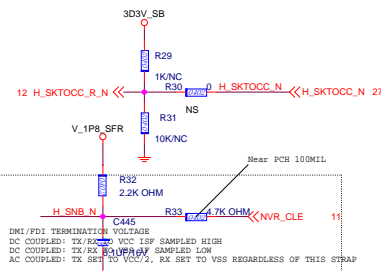
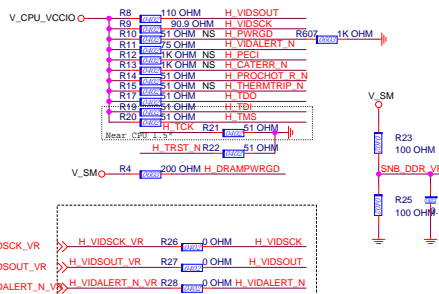
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Title			
Cover Sheet			
Size	Document Number	Sugar Bay	Rev
B			1.0
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DMT/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX VCC 18P SAMPLED HIGH  
DC COUPLED: TX/RX VSS 18P SAMPLED LOW  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

CPUG	H	L	DESCRIPTION
0	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED
2	NORM	REVERSE	PEGLANE REVERSAL[0], X16
3	RESERVED	RESERVED	RESERVED
4	RESERVED	RESERVED	RESERVED
5	+	+	PROPOSEL[0]
6	+	+	PROPOSEL[1]
7	RESERVED	RESERVED	RESERVED
8	RESERVED	RESERVED	RESERVED
9	RESERVED	RESERVED	RESERVED
10	RESERVED	RESERVED	RESERVED
11	RESERVED	RESERVED	RESERVED
12	RESERVED	RESERVED	RESERVED
13	RESERVED	RESERVED	RESERVED
14	RESERVED	RESERVED	RESERVED
15	RESERVED	RESERVED	RESERVED

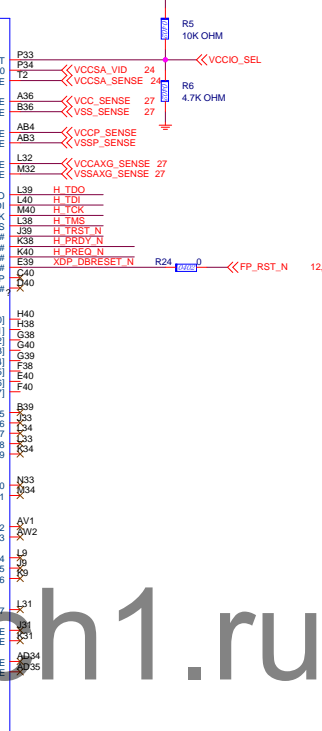
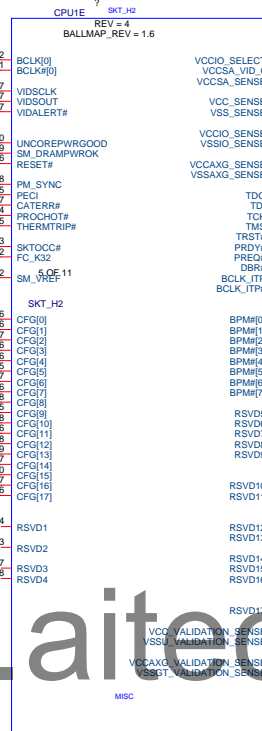
SNB STRAP TABLE

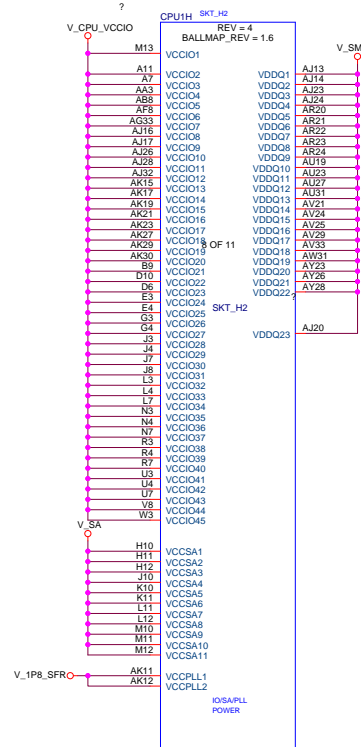
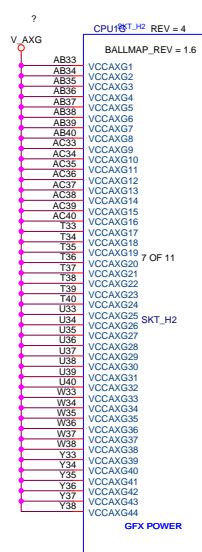
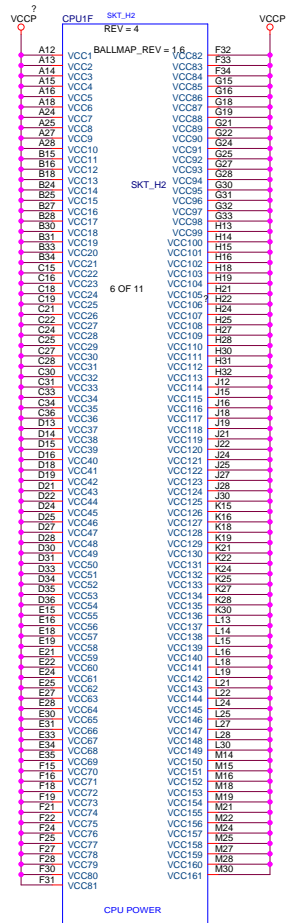
CPUG	H	L	DESCRIPTION
0	RESERVED	RESERVED	RESERVED
1	RESERVED	RESERVED	RESERVED
2	NORM	REVERSE	PEGLANE REVERSAL[0], X16
3	RESERVED	RESERVED	RESERVED
4	RESERVED	RESERVED	RESERVED
5	+	+	PROPOSEL[0]
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8	RESERVED	RESERVED	RESERVED
9	RESERVED	RESERVED	RESERVED
10	RESERVED	RESERVED	RESERVED
11	RESERVED	RESERVED	RESERVED
12	RESERVED	RESERVED	RESERVED
13	RESERVED	RESERVED	RESERVED
14	RESERVED	RESERVED	RESERVED
15	RESERVED	RESERVED	RESERVED

PEG CONFIG TABLE

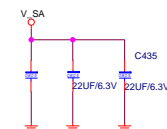
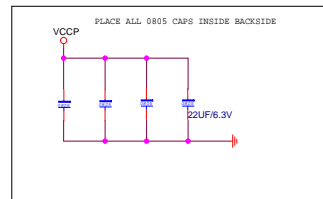
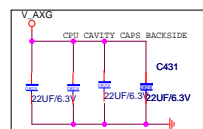
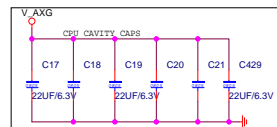
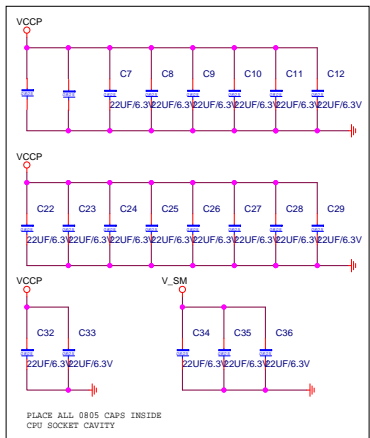
SEL1	SEL0	PCIE CONFIG
1	1	1X16 (Default)
1	0	2X8

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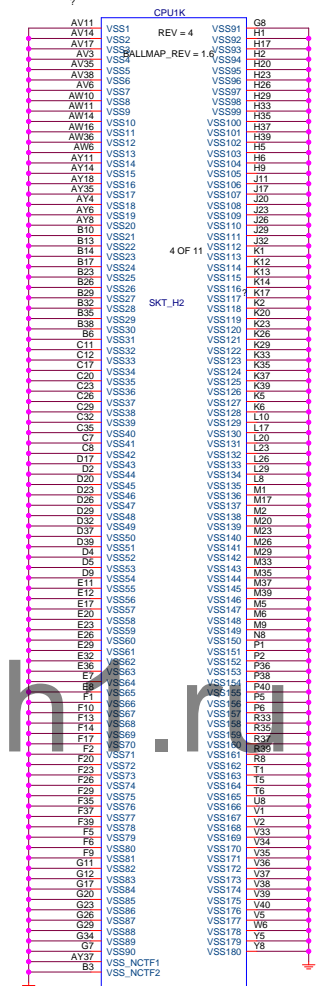
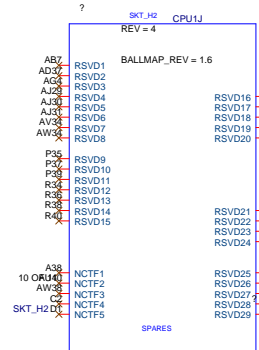
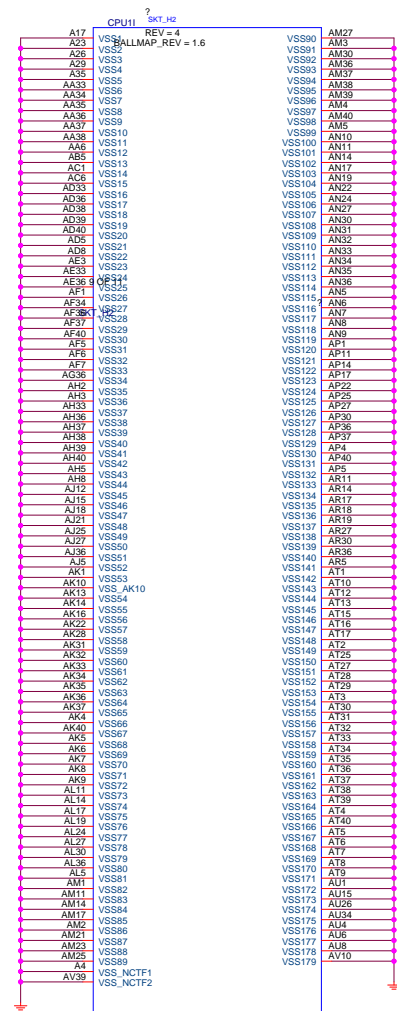




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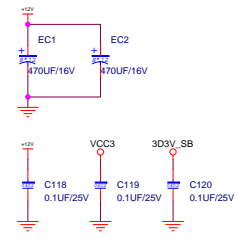
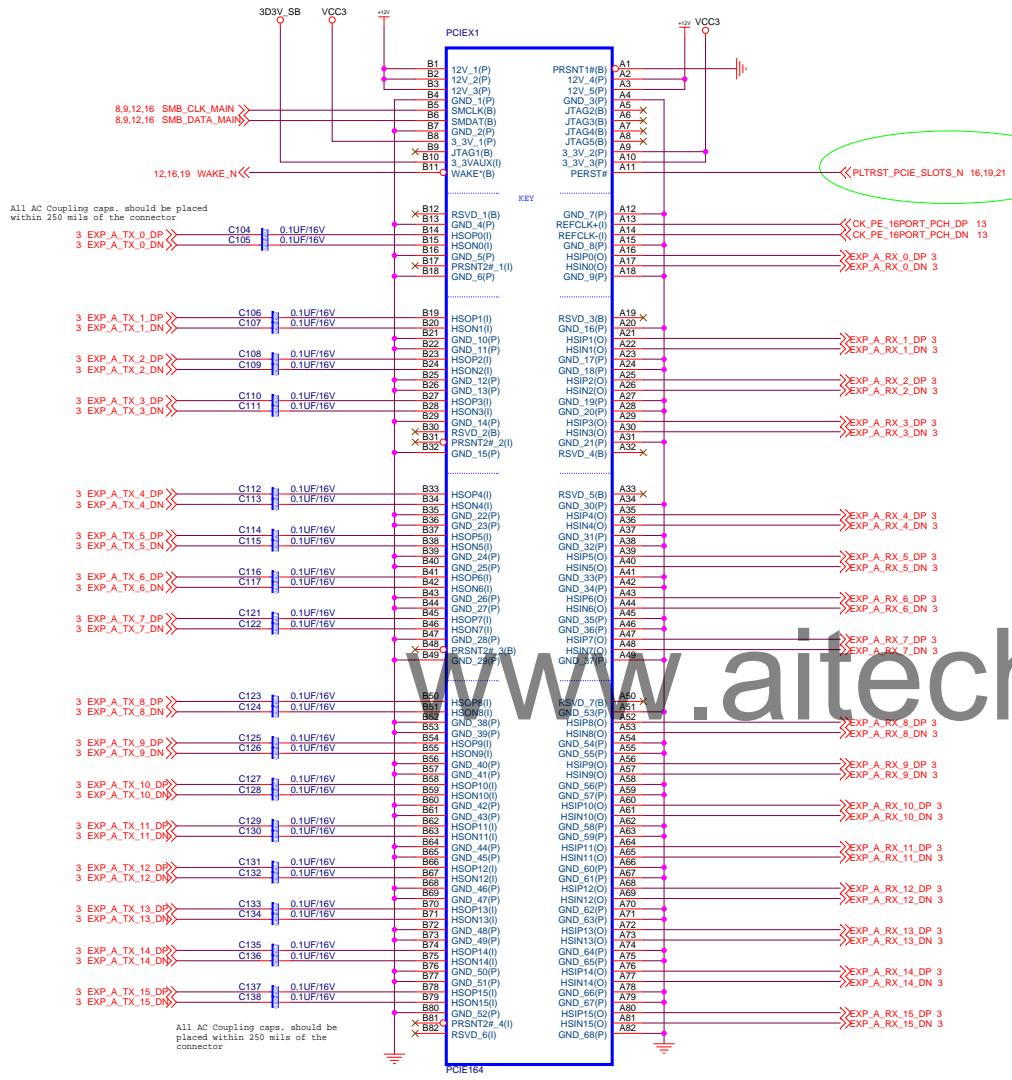


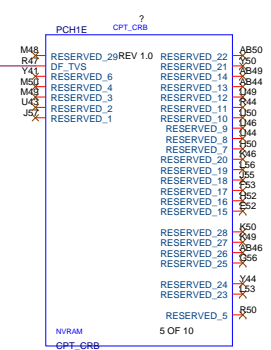
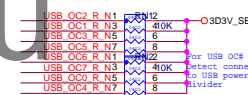
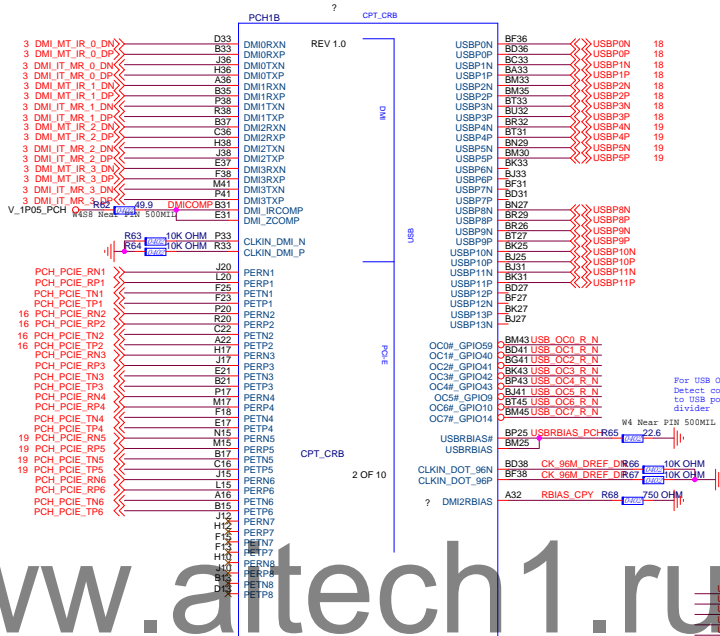
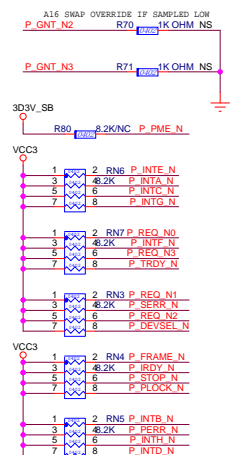
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21 PWRGD\_3V

R81 PCH MEPWROK\_R

PCH1C

REV 1.0

CL\_CLK1

CL\_DATA1

CL\_RST1#

PCH MEPWROK\_R BC46

APWROK

BM21

PWM0

PWM1

PWM2

PWM3

PCH GP17 PU BT17

PCH GP1 PU BR19

HEC GP6 BA22

PCH GP7 PU BR16

PCH GP6 PU BU16

TEST SETUP MEMB18

BOARD DIFF BR17

PCH GP7 PU BP15

BC43

PCH CONFIG JUMPER BA33

GP38 CRB DETECT BE54

GP39 GFX CRB DETECT BF55

SV ADVANCE GP48 AW53

AW53

CLINK\_SATA\_N

CLINK\_SATA\_P

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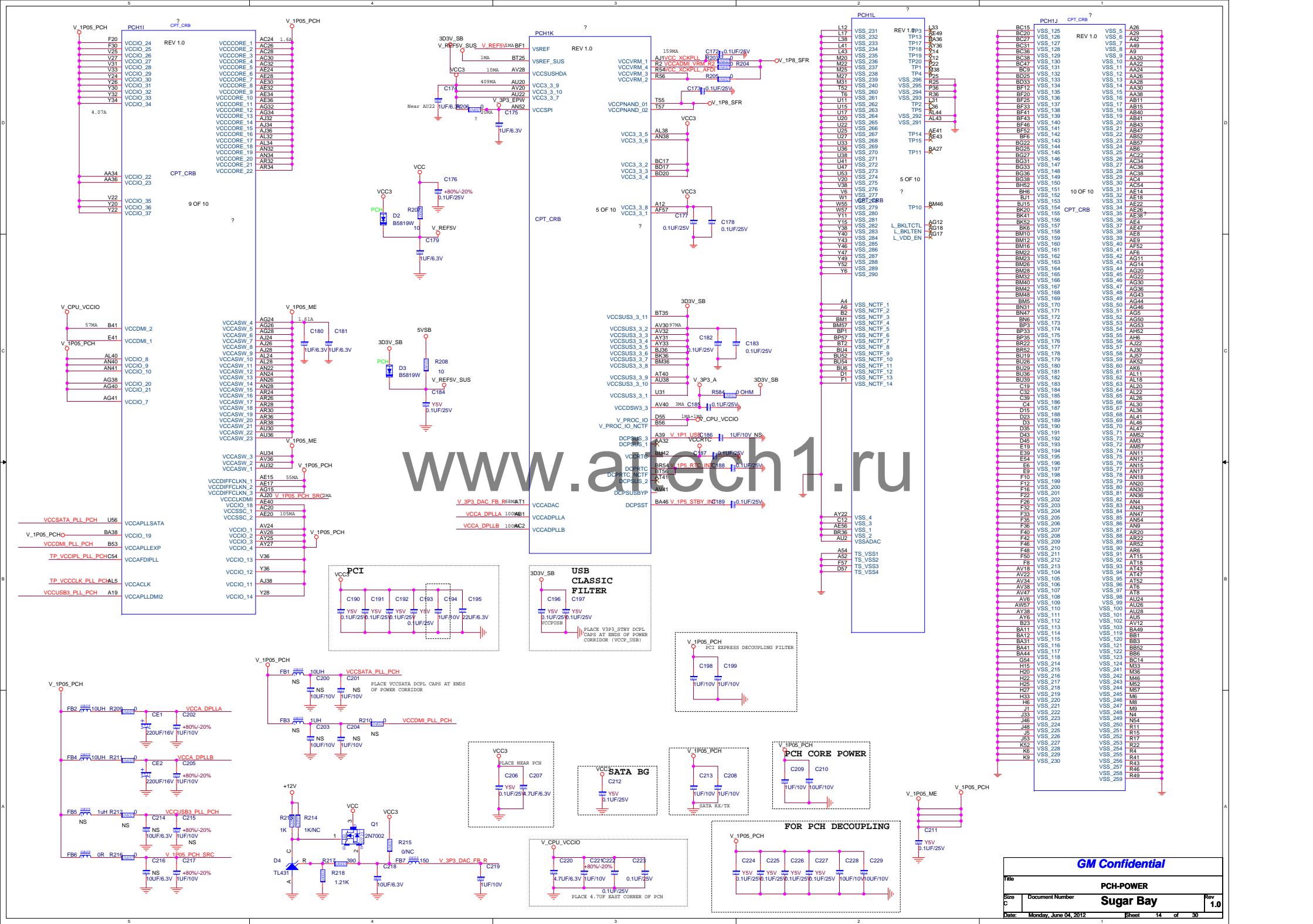
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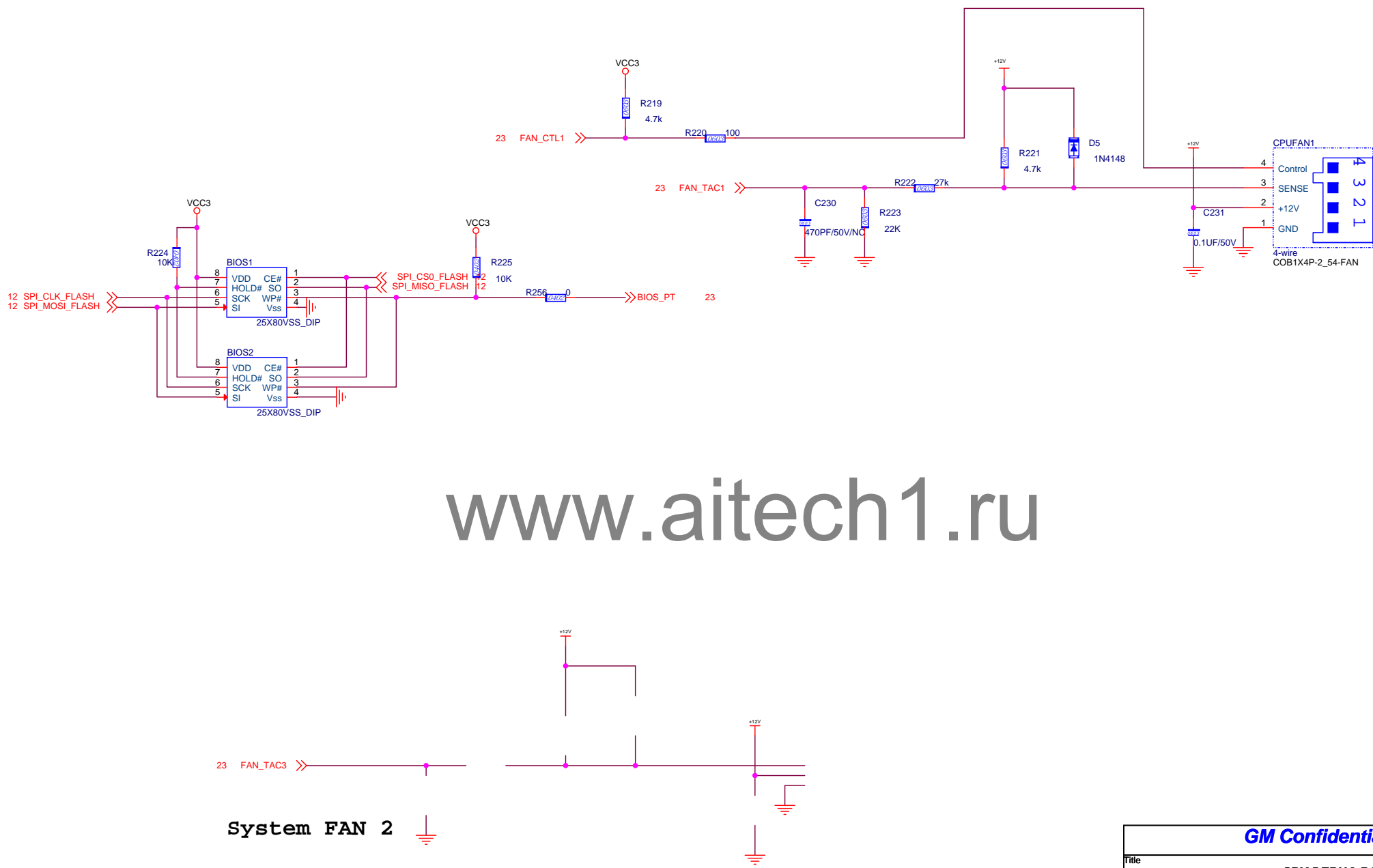
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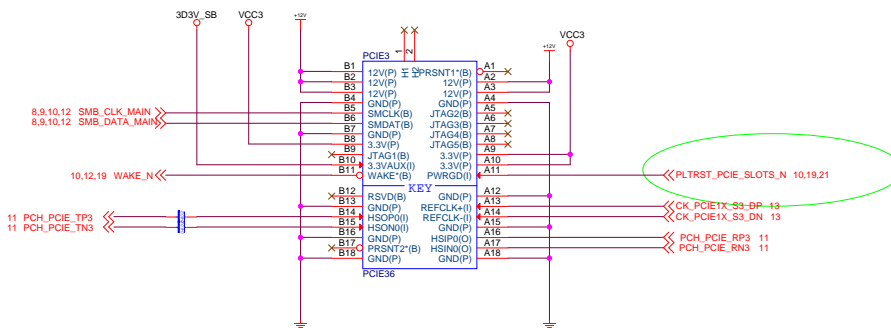
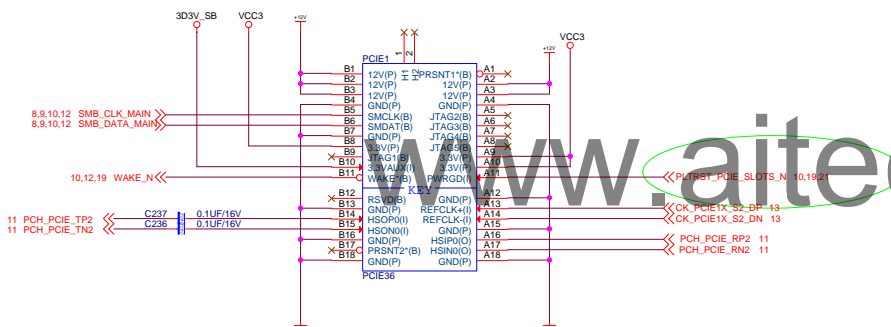
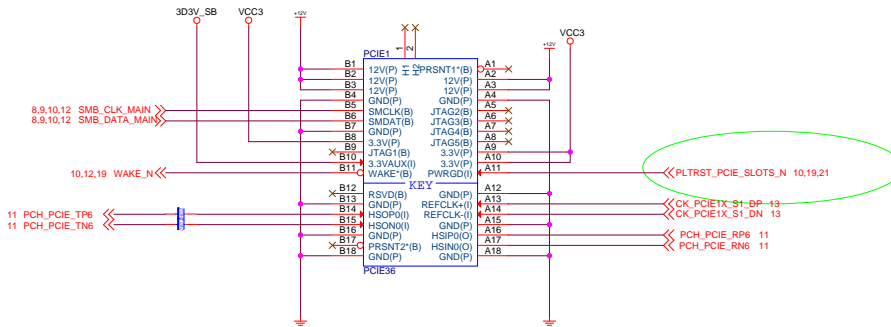


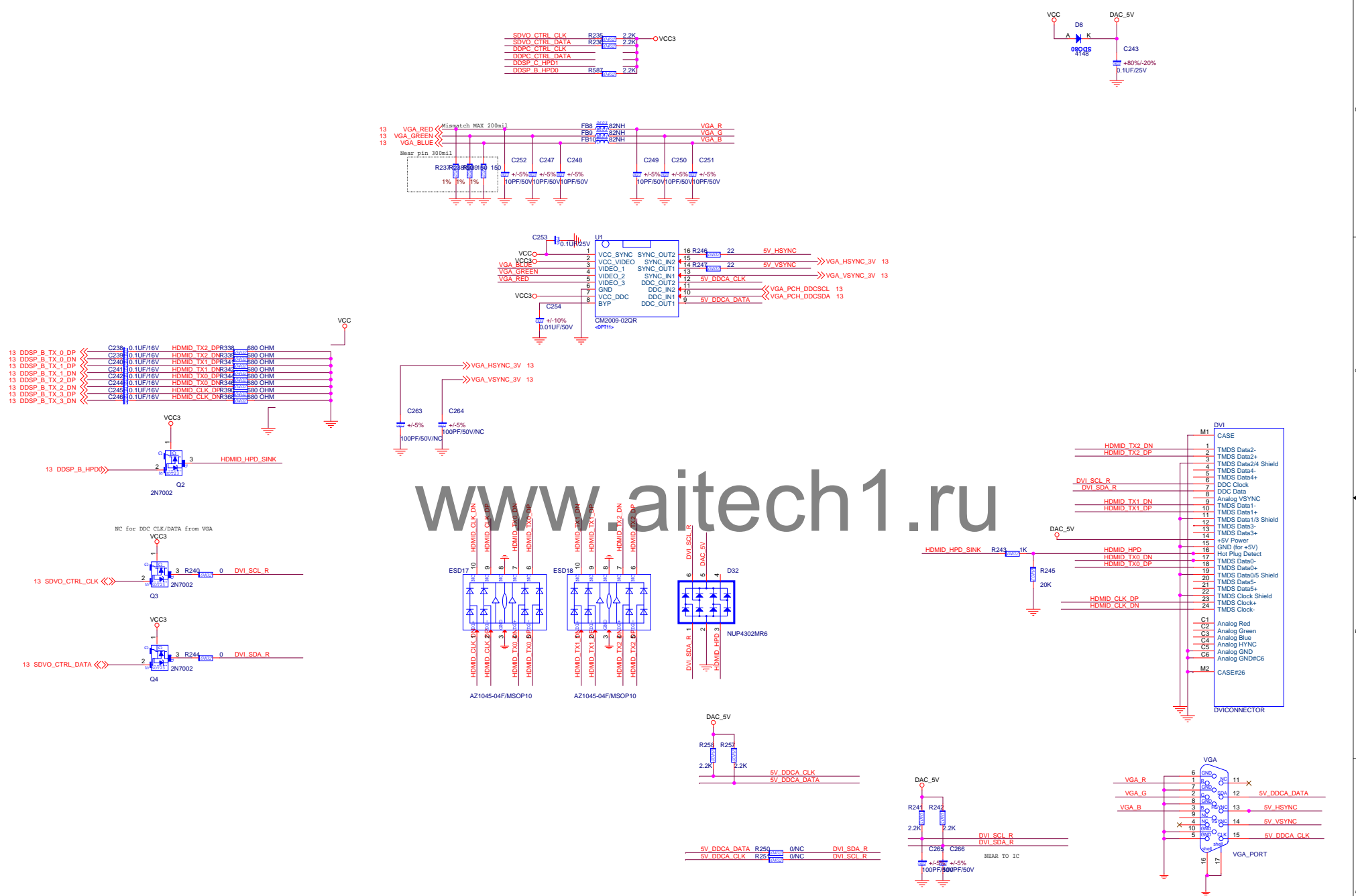




System FAN 2

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Title			
SPI&DEBUG PORT			
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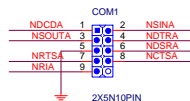
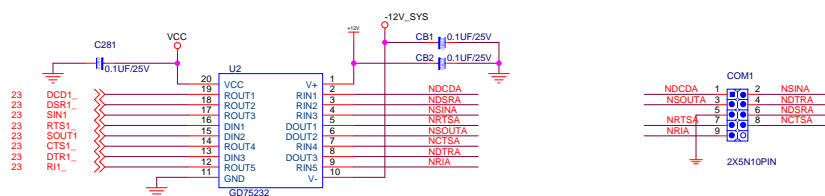
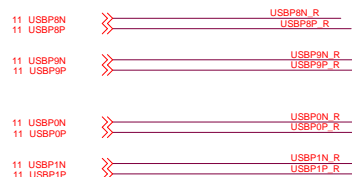
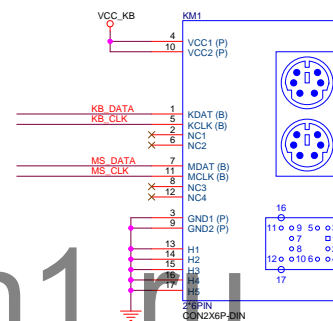
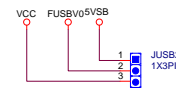
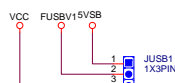
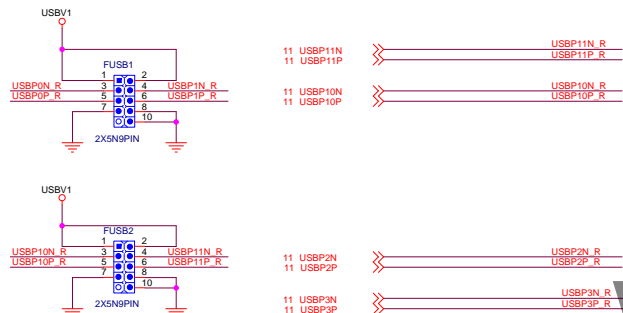
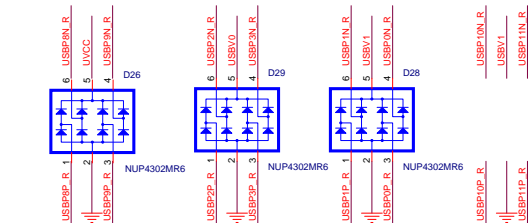
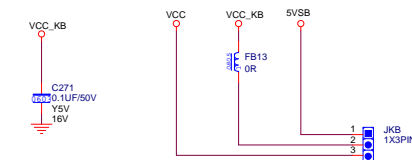
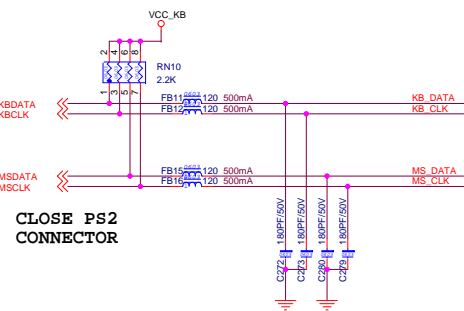
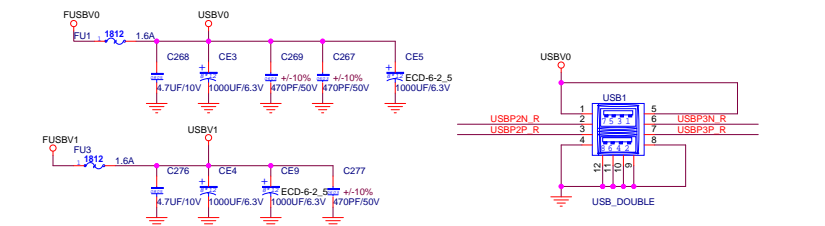




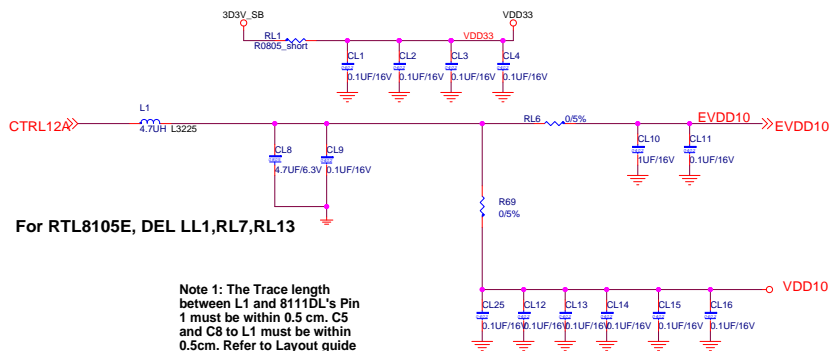
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Design Note: For DVI-I Support Please Use Port B See MOW WW07 For Detail.

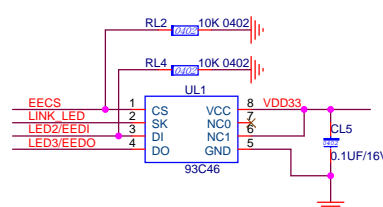
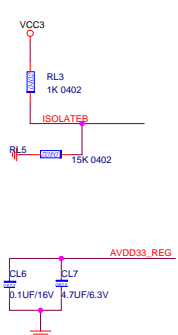
GM Confidential			
File	VGA/DVI/HDMI		
Size	Document Number	Sugar Bay	
C		Rev	1.0
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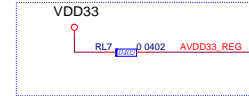
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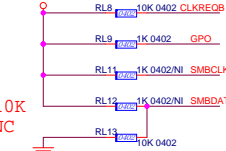
Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.



For RTL8111E, use this block

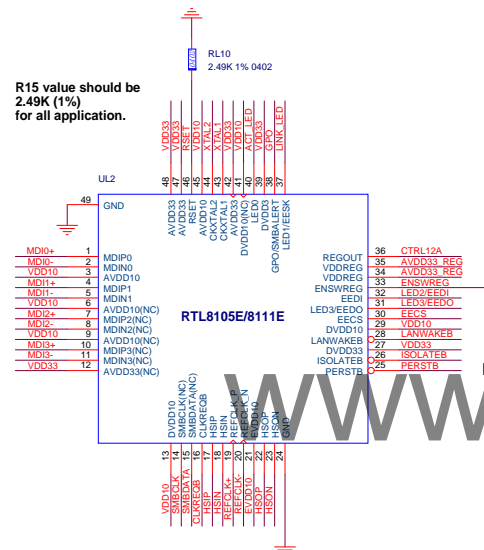


For RTL8105E, Del RL14, Add RL19

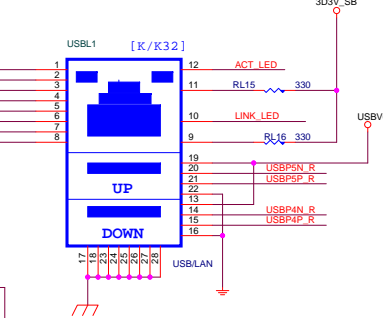
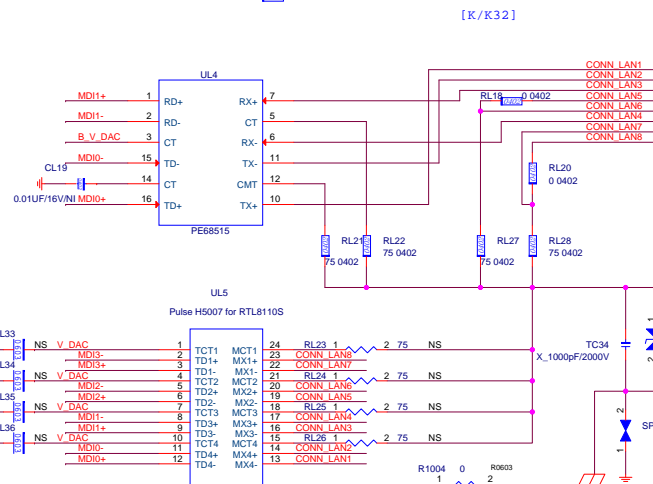
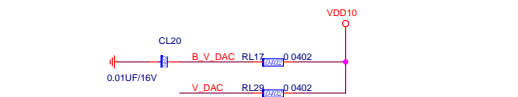
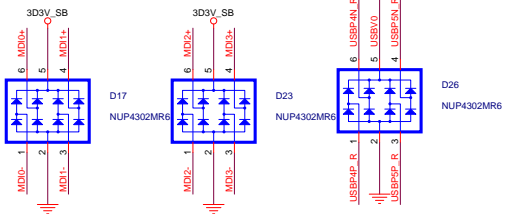
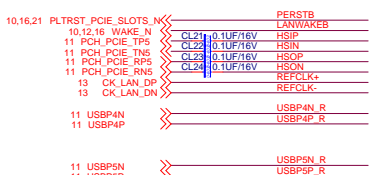


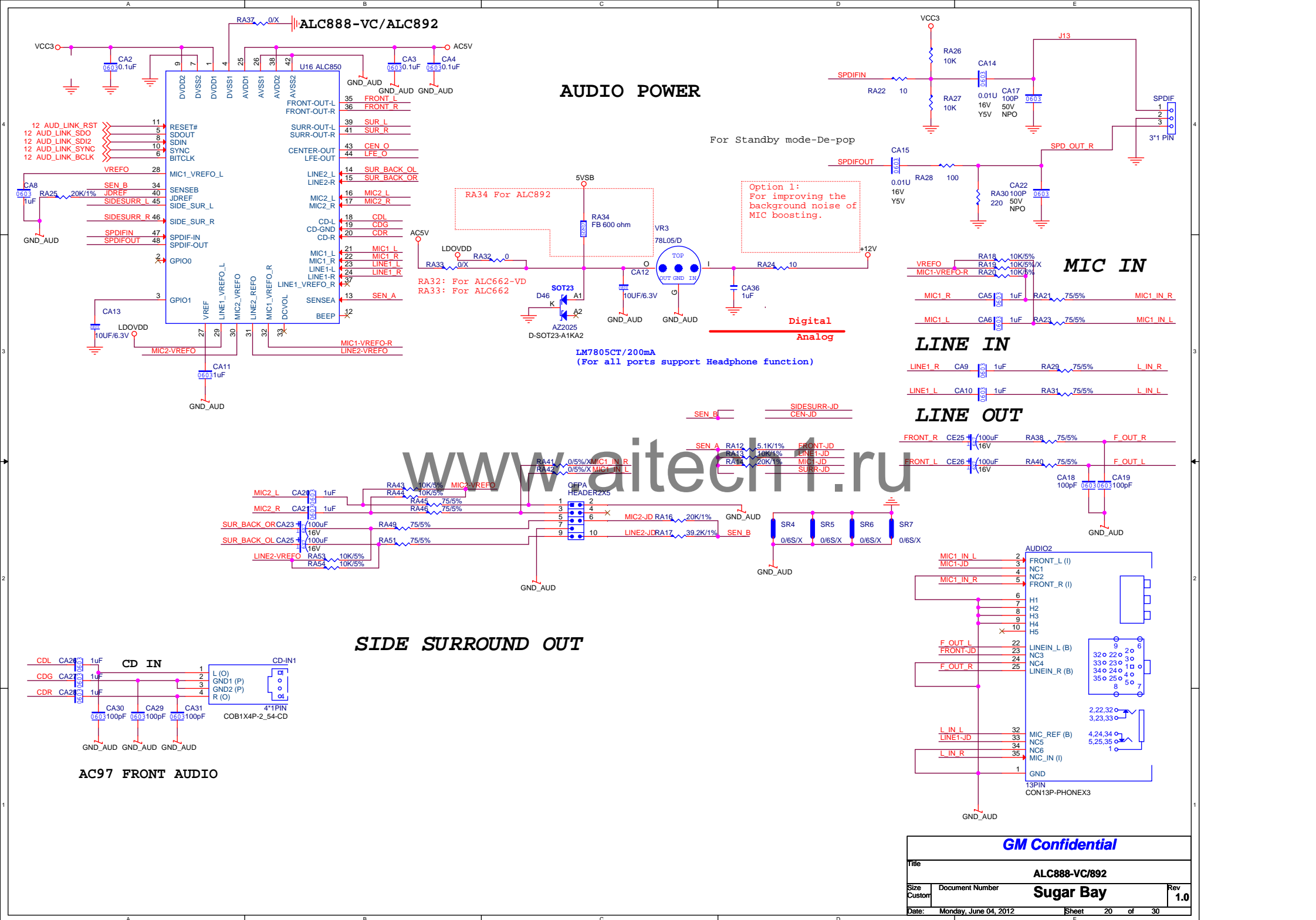
8111E RL13 10K  
8105E RL13 NC

R15 value should be 2.49K (1%) for all application.

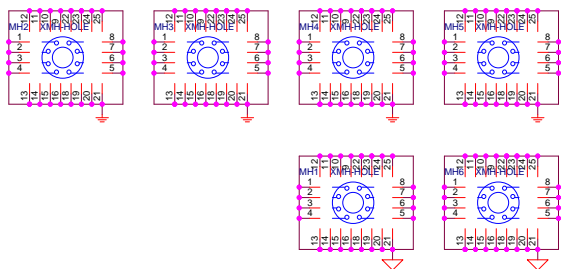


For RTL8105E, Del RL14, Add RL19









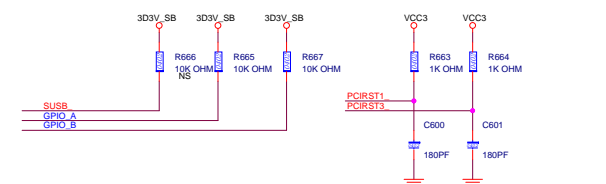
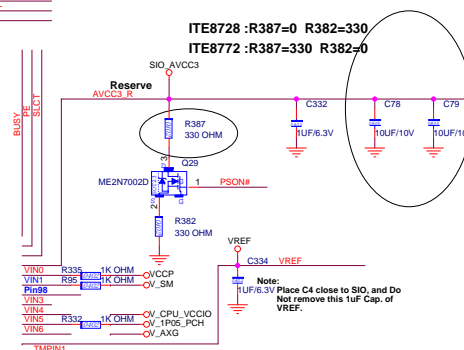
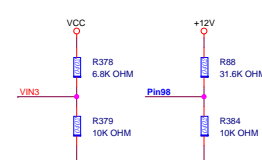
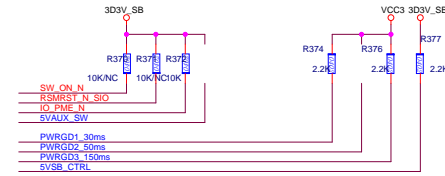
Symbol	value	Description
Jp3	1	Disabled.
Pin 124	0	Flash I/F Address Segment 1 is enabled
Jp4	1	K8 power sequence function is disabled
Pin 126	0	K8 power sequence function is enabled
	11	The default value of EC Index 15h/16h/17h is 80h
Jp5 & Jp6	10	The default value of EC Index 15h/16h/17h is FFh(Fan off )
Pin 124 & 46	01	The default value of EC Index 15h/16h/17h is 00h(Fan full speed)
	00	The default value of EC Index 15h/16h/17h is 40h

```

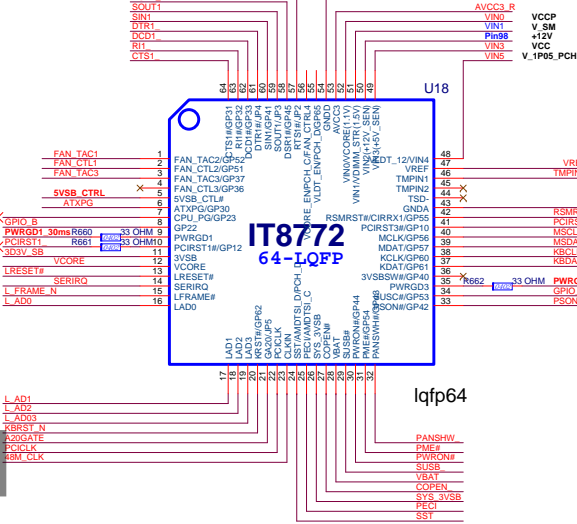
If without use these pins, Please
Don't let it floating
1.Pin 95:VIN3/ATXPG
2.Pin 71:SUSB#
3.Pin 3:PCIRSTIN#
4.Power On Strapping Options pin
5.Pin80-83 KCLK/KDAT/MCLK/MDAT

```

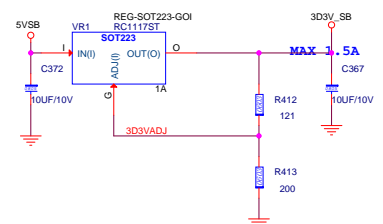
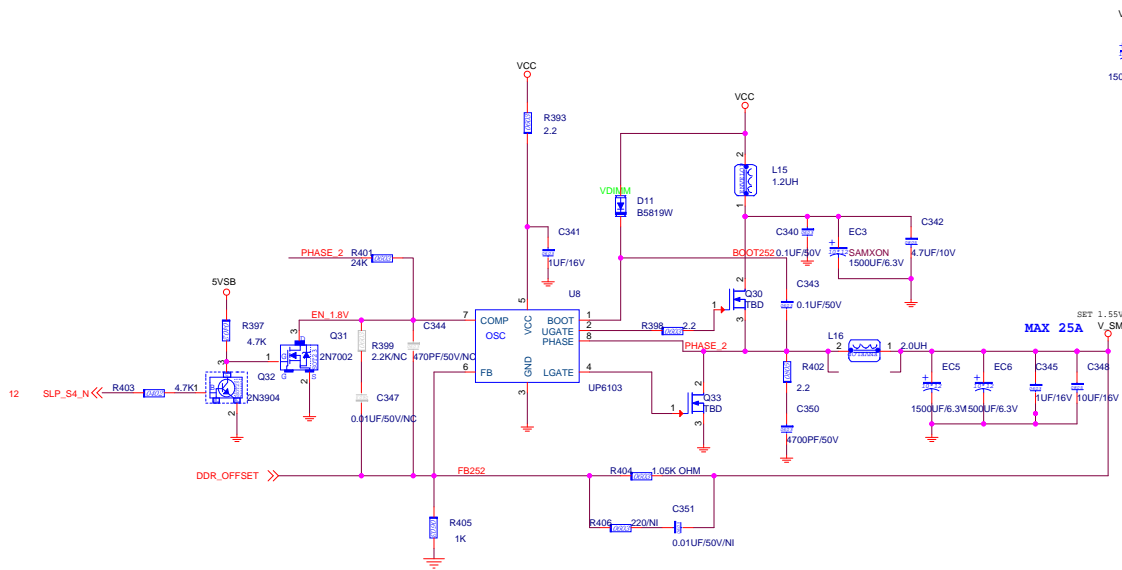
88	SIN1	SIN1
88	SOUT1	SOUT1
88	DSR1_	DSR1
88	RTS1_	RTS1
88	RI1	RI1
88	DCD1_	DCD1
88	DTR1_	DTR1
88	CTS1_	CTS1



## RT

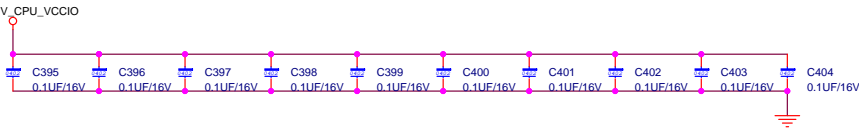
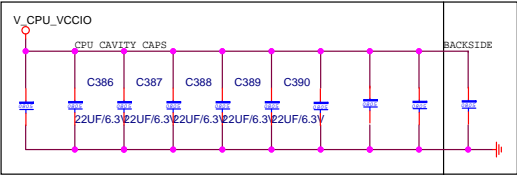
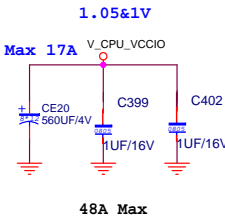
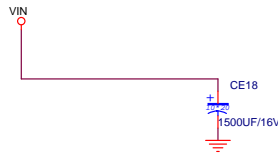


**P12页 KBRST A20GATE 上拉电阻R134 R137改为1K**



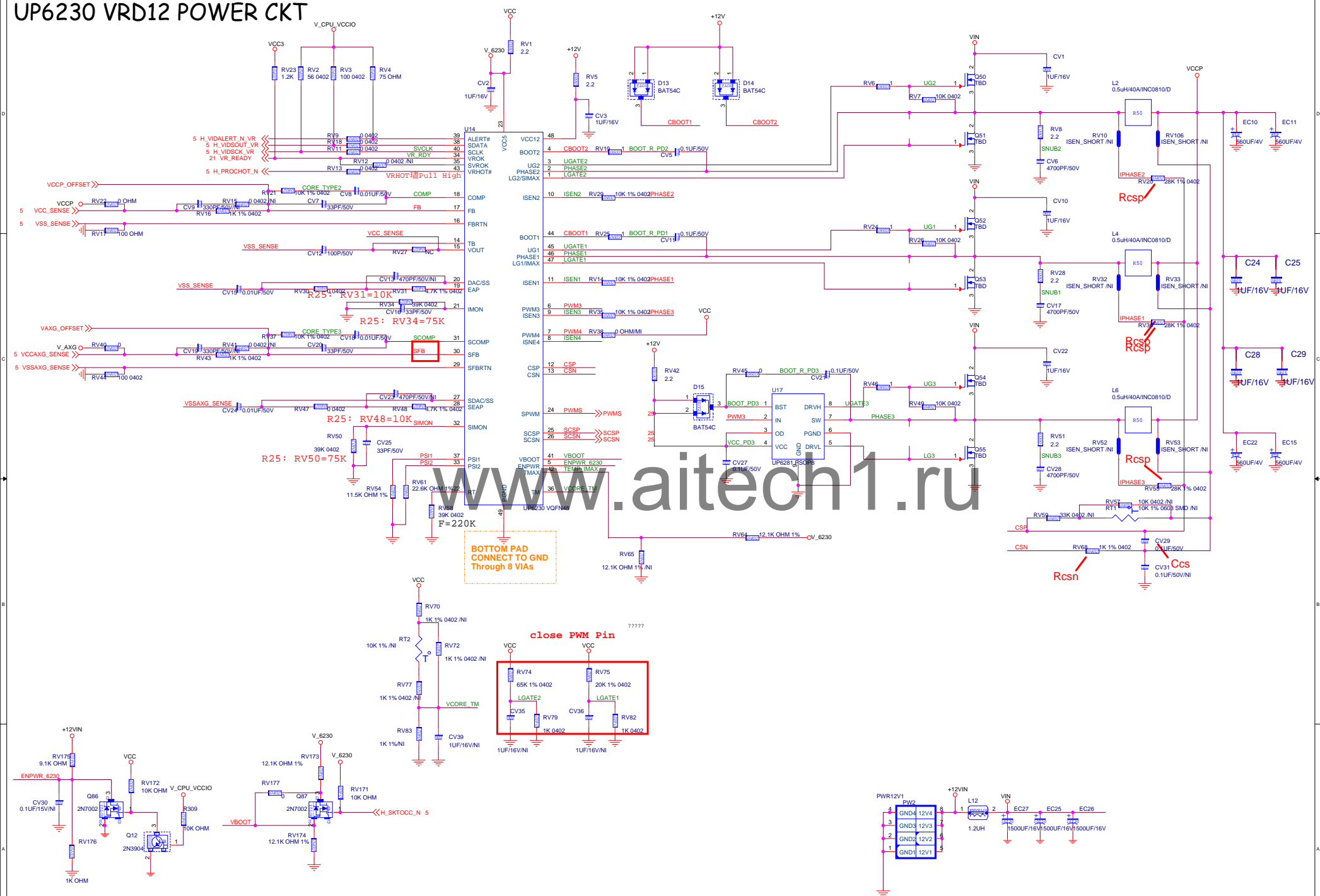


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## UP6230 VRD12 POWER CKT



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